ABSTRACT

A desynchronizer for desynchronizing one or multiple channels of SONET/SDH data signals, which includes a first in first out (FIFO) buffer having an input coupled to said data signals and an output for outputting asynchronous data obtained from one or more of said SONET/SDH data channels. An arithmetic unit coupled to the FIFO performs all operations required for single or multi-channel desynchronization. An endless phase modulator is coupled to the arithmetic unit and to the FIFO and is operative, in response to input from the arithmetic unit, to produce a single output desynchronized clock or multiple output desynchronized clocks.